## IN THE SPECIFICATION

Please amend the specification as follows:

DEG 4/10/07

The paragraph beginning at page 5, line 3 is amended as follows:

Figure 1 is a block diagram of a communications transceiver 100 according to one embodiment of the present invention. The communications transceiver 100 includes a link level protocol (LLP) 110, a driver 130, a canceller/equalizer 120, and a receiver 140.

The paragraph beginning at page 5, line 24 is amended as follows:

The driver 130 includes a driver circuit 134 and an impedance controller 132. The impedance controller 132 connects to driver circuit 134 via an impedance controller line 136. The impedance controller 132 continuously monitors the impedance of the communication channel by monitoring signals representing voltage, temperature, or other variation or process characteristics of the communications medium. The impedance controller 132 then interacts with the driver circuit to automatically drive a signal through the driver output 138 with an output impedance matching that of the communication medium. For more specific details on how the impedance controller works, see "Impedance Controller" U.S. Patent No. 6,703,908, Issued, March 9, 2004 ~~U.S. Patent Application Serial No. (Attorney Docket # 499.073US1)~~, which is incorporated by reference.

The paragraph beginning at page 6, line 23, is amended as follows:

In one embodiment, receiver 140 receives the equalized signal from the canceller/equalizer output 121. The receiver includes a receiver circuit 142 connected to the canceller/equalizer output 121, a clock receiver 144 receiving a clock signal 145, and a bit deskew 146 connected to the receiver circuit line 143 and the receiver line 116. As described in "System and Method for Adaptively Deskewing Parallel Data Signals Relative to a Clock" U.S.